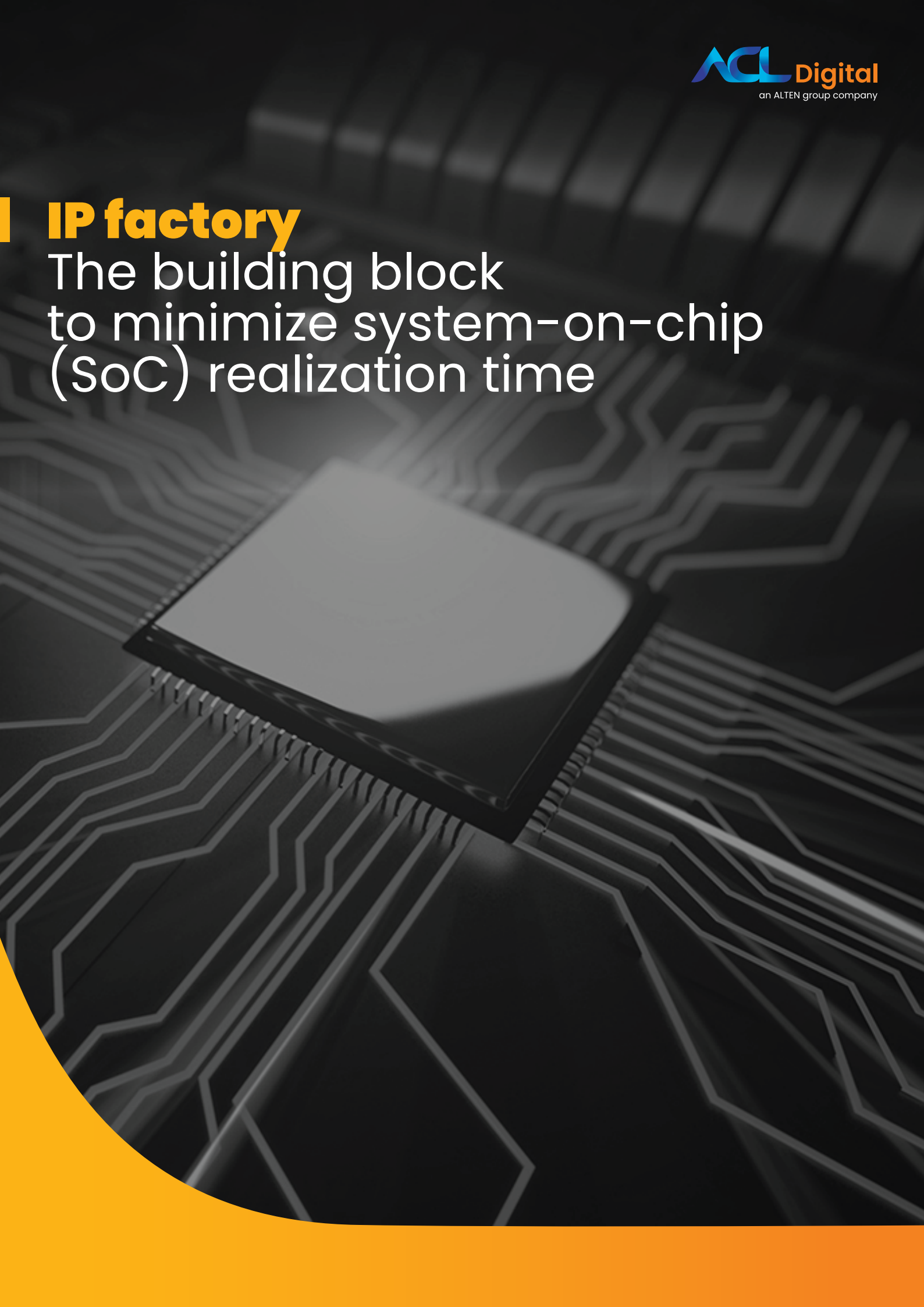
ACL Digital
an ALTEN group company

IP factory

The building block to minimize system-on-chip (SoC) realization time



In this era of automation, highly complex and customized multifunctional chips are required in every sphere of life. In parallel, as the semiconductor industry has evolved over the years making a shift from very large scale towards super large-scale integration, the design complexity has exploded. This ever-increasing scale and scope of semiconductor devices in today's global market calls for a significantly greater design effort.

This in turn, has led to the search for methods to stop the development cycles from growing exponentially. Apart from being a best practice, design reuse has also become the main tool and a critical necessity to tackle this situation. To integrate multiple functionalities on a single chip, pre-designed IP blocks are of utmost importance as these customized designs enable leveraging of proven components.

What's next in the IP Factory development?

In addition to the design effort, the implementation tasks of these have also become far more complicated. The shrinking geometries have imposed stricter regulations on the design hardening, with increase in cost of manufacturing manifold and reduction in silicon tolerances to obtain reasonable yield margins. The need for building silicon around proven cores has therefore become an indispensable task to build confidence towards the overall product realization.

The utilization of existing hardware components is now one of the main methodologies to ensure timely and cost-effective deliveries. The push to reutilize the efforts spent in creating proven silicon is complicated by many factors. One of the factors being the increasingly differentiated applications which has led to a greater spread of technology node offerings as foundries create a graded scale to enable cost/performance trade off during design implementation. This means that derivative usage inevitably lands on a different node, where even if the divergence is minor, the original IP may not be used as is.

Further different design contexts often require marginal changes to either the IP, or the collaterals around them, or both, before they can be effectively reused. These factors create a compelling need for a solution where the existing IP is transitioned to the end use scenario while preserving the existing performance confidence. To ensure the efficiency and performance of the transitioned IP for a specific scenario, one of the major challenges is to validate the IP by testing it with a large number of test patterns in a real system environment using real software.

While the IP vendors and internal teams with design houses step up to meet these challenges, the dynamic scenario, which is the hallmark of the industry, means that additional support is needed. There exists a requirement for an ecosystem where reliable partners exist to add momentum towards the said conversion. The partners in such an ecosystem are expected to work as an extended team, but independently, adding bandwidth. Ideally, they would be a complete factory where the requirements can be incorporated, and the finished product being obtained with the specified parameters.

ACL Digital's Approach to IP Factory

At ACL Digital, we believe in the fundamentals first approach towards building the complete solution. In tangible terms, this means creating and honing skills starting from the foundational pieces of analog and digital layout to flow infrastructure continuing up to access of cutting edge foundry technologies. Our philosophy is to work with our customers as their partners, to be able to fulfil any requirements that they might have from the smallest resource augmentation to being able to support them with a completely outsourced turnkey solutions spanning the entire gamut from specification to final characterized silicon. We aim to provide customers with end-to-end, scalable solutions to assist them in their goals, with the flexibility of taking on the simplest to the most complicated tasks. We put a great emphasis on dependability and transparency as we go through the execution cycle, providing for complete view of the progress even as we work toward guaranteed first pass success and on time deliveries.

We endeavour to provide a single stop solution for all the customer requirements related to an IP factory, and to that end we are continuously and proactively building partnerships with foundries and IP vendors to maintain our technological edge with access to cutting edge nodes and the best in class IP knowledge to help our end customers. Whether the customer aims to develop custom IP for product differentiation or wants a rapid porting of libraries on a new process node or a PDK flavour we have the experience and expertise to help. Transitioning complex analog mixed signal IPs to cutting edge node at lower geometries is yet another focus area along with proving the same through test chips.

Key elements of IP Factory

Towards the realization of our philosophy, the ACL Digital IP factory is built to be flexible and scalable, and is based on three technology pillars as below:

- A foundation IP portfolio of CAD proven reference designs across technologies which provide a strong starting point enabling the project to get off the ground quickly
- A custom design flow from spec to GDS, enabling rapid bring up, characterization and modelling of circuits and IPs across a full range of operating corners for multiple libraries
- An expertise in cutting edge technology nodes, with currently active efforts going down to 5nm even while providing for a spread all the way up to 180nm

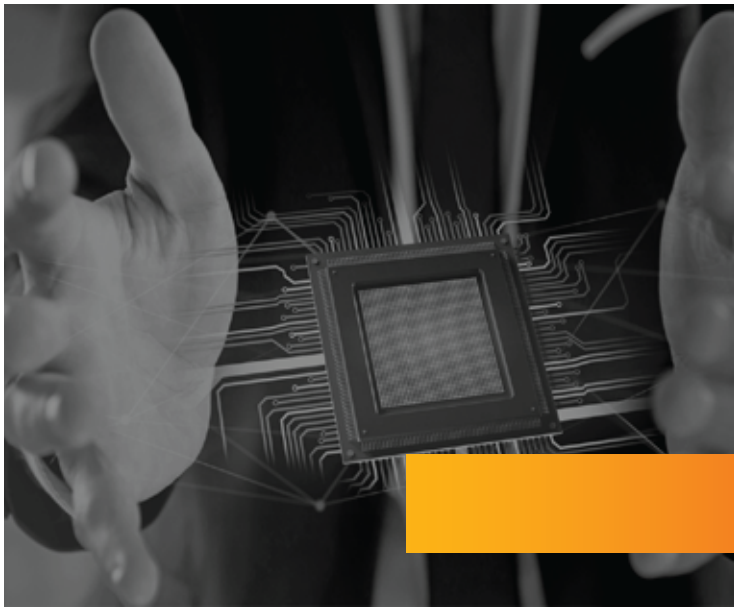
These foundational pieces support our offerings in a circuit design, layout and characterization space. In addition, they also enable our services towards porting analog, digital and AMS circuits as well as the ability to take IPs all the way from specification up to silicon characterization through our test chip offerings. Our services encompass the entire spectrum of requirements that a customer may have from an IP factory, and can be segmented into the following main areas:

- **Custom Embedded SRAMs:** Development of Single port, Dual port, Register files, ROMs from specification to GDS
- **Analog & Mixed signal:** Development of AMS components such as PMIC block Data Converters, High speed IOs, from specification to GDS
- **Standard libraries:** Cell libraries development
- **Layout migration:** Layout development of complex custom circuits such as USR SerDes Tx and Rx blocks, as well as digital designs
- **IP Test Chips:** Test chip design and layout targeted for IP silicon testing i.e. SRAMs, SerDes, DDRs. Enabling silicon correlation with design and functionality checks

Between these, our offerings cover the complete set of requirements typically needed for obtaining a robust reusable IP core.

Benefits of IP Factory and Conclusion

Working with ACL Digital's IP factory provides for effective realization of the concept of design reuse. The IP factory makes it possible to have a trustable implementation of high-confidence IP as per the new requirements. The IP factory approach enables immediate availability of specialized teams driving lower program latency. Solutions and products to get the implementation off the ground can be easily accessed resulting in TAT reductions. These advantages are achieved even with the need for customization for power, performance or area as required. It is a weapon in the arsenal that just cannot be missed out on.

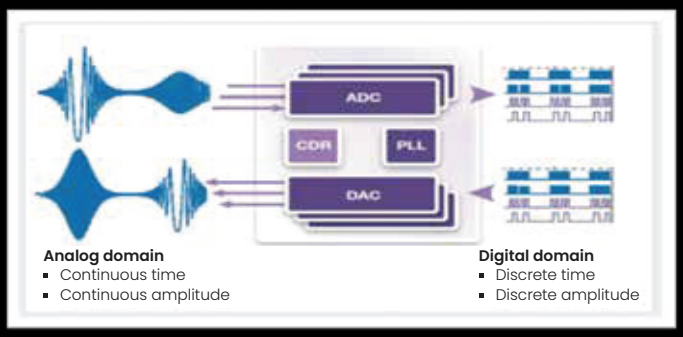


Our success stories

1 Analog layout porting factory: ACL Digital's analog layout centre excels in cutting edge nodes, supporting offshore development for tier 1 marque semiconductor houses. The CoE handles design, layout and characterization of analog circuits and IP sub blocks.

Analog Layout Center of Excellence

Customer	American Semiconductor company that develops computer processors & related technologies.
Nature of Engagement	Offshore Development Centre in Bangalore with Surveillance & Firewall. 3-way NDA between ACL - Customer - Foundry for a leading - edge node.
IP Portfolio	USR SerDes, Data Converters, Clock Circuits, Power Management Block, High Speed las, DDR sub-blocks
Team Size	25 Layout resources and few circuit design folks



AMS and CAD

USR SerDes Tx and Rx:

Layout development of SerDes blocks at 5nm technology node.

- Offshore development centre with 3- way NDA between ACL – Customer - Foundry for 5nm Tech access
- Scratch layout development: floor planning, power mesh template, EM/IR fixes etc.
- Development of IP sub blocks, test chip implementation i.e. bump placement, top level sign offs etc.
- Integration of IP over SoCs

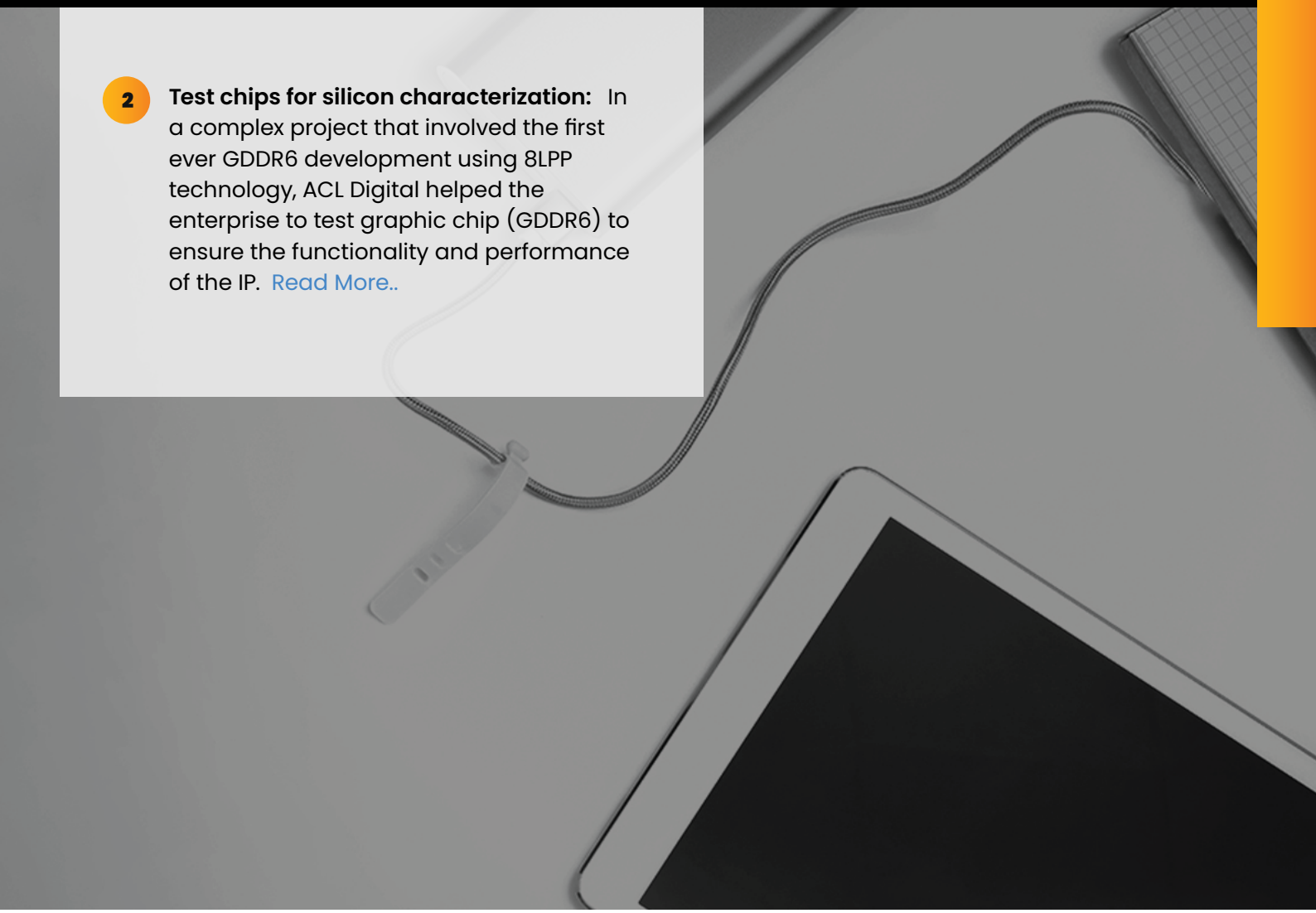
PMIC/DC-DC Converter:

Design for PSoC battery mode at 180nm.

- On Chip 3.3V generator with power supply monitor(POR, LV detect)
- POR, PSM, relaxation oscillator implementation
- Design delivery from Spec to GDS

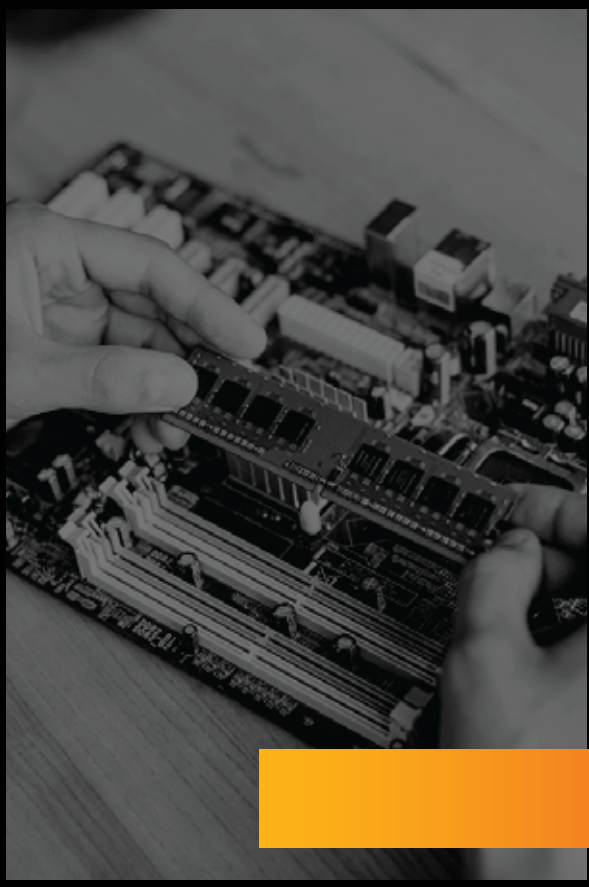
Spice test structures for future technologies:

- Test structures implementation for future advances technologies
  - On silicon characterization of followings:
- NMOS, PMOS, Inverter chain, MOS capacitor, capacitor/resistors, memory bitcell, PAD design for PDK qualification
- PCELL generation flow to generate, place and to connect to PADs for various spice structures.



2 **Test chips for silicon characterization:** In a complex project that involved the first ever GDDR6 development using 8LPP technology, ACL Digital helped the enterprise to test graphic chip (GDDR6) to ensure the functionality and performance of the IP. Read More..

3 **Custom memory development:** ACL Digital takes novel approaches to create SRAMs targeted for dynamic power reduction and development of compiler built around a unique architecture customized for enabling high speed memories.



End to end development of SRAM's, ROM and RF's

- Developed Single/multi bank SRAM's, Dual port SRAM's, Pseudo dual port, Registers files and NAND based high density ROM
  - SRAMs targeted for high-speed, ultra low power and high density
  - Various SRAM architectures i.e. Multibank, butterfly, paging , sandwich
  - Various SRAM features i.e. power switches, redundancy, Scan, BIST, dual rail power, retention till access etc.
- Experience in technology nodes from 4nm to 180nm across various foundries

Memory Compiler development

Inbuilt compiler flow which supports:

- Netlist tiling (Netlister), GDS tiler
- Automated simulation flow for char and margining
- Liberty generator with curve fitting
- FE generator, views generator

Layout automation

- Skill based Platform to automate various spice structures using Pcell approach

Low power SRAM compiler:

Overview: A noval approach of integrating inductor with digital circuits for Energy Recycled SRAM targeted for dynamic power reduction. The developed SRAM functionality with inductor added in Read and Write "VSS" path with the on-fly pulse calibration circuit to control the resonant period for the optimized dynamic power saving.

Key Features

- First SRAM with integrated inductor
- New approach of designing self-time path to control the signal flow with inductor in place
- Process node : 28nm HPC+, Power supply : 1V

Benefits

- 30-40% reduction in SRAM dynamic power
- Self Debugging capability and DMA enablement for Test Chip
- Easy integration

High speed SRAM compiler (L1/L2 cache):

Overview: Enablement of GHz memory at 65nm Technology node. Developed compiler with a unique architecture customized for high speed.

Key Features

- Designing of CLK2WL and BL2Q paths in minimum possible stages, IO design with reduced load on bitlines
- Multibank architecture and layout optimization to support Mux-1 architecture
- Process node : TSMC 65nm LP , Power supply : 1.2v

Benefits

- Enablement of SRAM with 990ps cycle time and 910ps access time

ACL Digital is a design-led Digital Experience, Product Innovation, Engineering and Enterprise IT offerings leader. From strategy, to design, implementation and management we help accelerate innovation and transform businesses. ACL Digital is a part of ALTEN group, a leader in technology consulting and engineering services.

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