ACL Digital
an ALTEN group company

CPU/CPU-Subsystem

High-Performance Computing (HPC) solutions combined with traditional desktop CPUs and specialized storage and connectivity resources into a large computing cluster can jointly solve problems beyond standalone computing architectures' reach.

ACL Digital Center of Excellence (CoE)

Traditionally, HPC implementations have been expensive to build, use and maintain. The economies of scale available with the burgeoning development of purpose-built, high-performance chips (CPU, GPU, FPGA) are beginning to drive HPC scale opportunities down the market with hyper-scale public cloud providers such as Amazon and Google and offer approximate capabilities on per user basis. These market dynamics are driving tremendous challenges to these engineering communities. ACL Digital has been working closely with several HPC players, AI, and Automotive, augmenting design knowledge.

ACL Digital's RISC-V Expertise in HPC Domain helps clients jumpstart RISC-V Core Design and SoC Development

- RISC-V SoC Design partner of an existing TSMC Client
- RISC-V Architecture definition (Both Micro and Macro), SoC Design, Integration, Core Verification, Physical Implementation
- RISC-V competency center with teams spread across the US and India

For Start-Ups, ACL Digital offers a complete package of end-to-end design support teams from Architecture to Tapeout and IP availability for all critical system IPs.

- Quick ramp-up of resources with multi-functional skills in near and offshore locations
- Availability of high-speed peripheral IP for SoC designs
- Setting up flow for physical implementation from the ground up based on TSMC advanced technologies (16nm to 5nm FinFET)

For Large OEM

- Hardening of ARM and RISC-V Cores for HPC designs
- High-end Processors (5.5 GHz)
- A9/A53 Core Hardening Experience (Custom flows depending on PPA targets)
- Redundant Cores in Lock-Step mode
- A9/A53 subsystem hardening with clock synchronicity (1.2GHz)
- RISC-V CPU-based solutions Architecture, Design, Verification

Our collaboration with industry associations To elevate customer experiences

RISC-V®
A Strategic Member of RISC-V

ARM®
ARM Approved Design Partner

ACL Digital Value Offerings

We executed multiple CPU-based SoC designs in a delivery ownership environment, including design, integration, verification, DFT, and physical implementation.

IP/CPU Architecture, Design, and Verification

- Fully scalable and configurable CPU core RISC-V
- 2 instructions per cycle in a single thread, multiple threads per core; multiple cores in a cluster; multi-cluster designs for RISC-V
- NOC, Debug, and trace features
- SoC fabric, memory controller, Functional Safety designs for Automotive caches
- Instruction set verification, Random Instruction Sequencing (RIS), and testing
- Assembly verification, Model development for RISC-V
- Cache coherence, memory ordering and consistency, prefetching, branch prediction, renaming, speculative execution, and memory translation
- High-speed interface sub-system integration
- SoC level debug ability enablement as an option through the Trace interface of the CPU architecture
- Power-aware CPU designs where the Cores/Clusters could be shut off during idle periods

SoC Design and Verification

- Standard verification components like SoC level Driver, Monitors, Reference Models, Functional Coverage and Top-level Test Bench, Scoreboards/Checkers/Assertions
- Processor-based SoC; configuration of the whole SoC or its sub-modules using the processor to drive SoC level stimulus
- Reusing the legacy test case scenarios with modifications for similar SoC functionalities present in its previous version
- Printing with user control verbosity, switching ON the required sub IP level messages; enabling debug switches of the verification methodology which will help to quickly debug RTL as well as the test bench/VE (Verification Environment) issues at SoC level
- Building verification environment for emulation platform and supporting simulation and verification of software functionality prior to SoC tapeout

SOC Physical Implementation

- 100+M Gates, 162Mbits of RAM, multiple instances of 8 channel multi-protocol SerDes, Two 72bit DDR3 @ 1866
- Flip chip bonding and package route aware IO packing
- Partitioning, Pin assignment, channel definitions and sizing, Timing budgeting
- Switchable domains
- Handcrafted Clock Implementation scheme to contain skew and divergence
- Drive strength/net-length configurable clock padding scripts to achieve uniform clock RC
- Multiple asynchronous crossbars on the chip
- Clock synchronicity aware channel assignment
- Intelligent “timing budget aware” pipeline register placement
- “Crosstalk and timing budget aware” staggered buffering strategy on channels
- Custom clock tree build to meet 1866 DDR “skew + divergence” and “duty cycle distortion” targets (64-bit Data, 8 bit ECC)

ACL Digital is a design-led Digital Experience, Product Innovation, Engineering and Enterprise IT offerings leader. From strategy, to design, implementation and management we help accelerate innovation and transform businesses. ACL Digital is a part of ALTEN group, a leader in technology consulting and engineering services.

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